

Clean Set of Amended Claims

1. (Twice Amended) A test circuit for a microcontroller unit, comprising:

an input circuit that comprises,

a first pin receiving a first signal, and

a second pin receiving a second signal; and

5 a test signal generating circuit that generates a test signal in response to a logical combination of the first signal and the second signal, wherein the test signal generating circuit comprises,

a counter that is enabled and disabled based on the first signal and the second signal, wherein the counter uses the second signal as a counting signal when enabled, and

10 a decoder that outputs the test signal when a count value from the counter reaches a prescribed count value.

2. (Twice Amended) The circuit of claim 1, wherein the test signal generating circuit comprises a logic circuit that logically processes the first signal and the second signal, wherein the counter is enabled and disabled based on an output signal from the logic circuit.